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Low Power and Area Efficient System Achieved by using Efficient Virtual Channels on Network on Chip

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Abstract

In network-on-chip (NoC), the data transferring by virtual channels can avoid the issue of data loss and deadlock. Many virtual channels on one input or output port in a router are included. However, if the router includes five I/O ports, then the power issue is very important in virtual channels. In this paper, a novel architecture, namely, smart power-saving (SPS), for low power consumption and low area in virtual channels of NoC is proposed. The SPS architecture can accord different environmental factors to dynamically save power and optimization area in NoC. Comparing with related works, the new proposed method reduces 37.31, 45.79, and 19.26% on power consumption and reduces 49.4, 25.5 and 14.4% on area, respectively.

Keywords: *Network on chip (NOC), smart power saving (SPS), system on chip (SOC)*

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INTRODUCTION

In recent years, the 3-dimensional IC and TSV (Through-Silicon Via) technology are proposed to solve area issues. The 3-dimensional IC of Intel Ivy Bridge processor and the 16-core multicore architecture can be implemented in 22 nm. Therefore, the multicore and heterogeneous systems are popular research in SoC (system-on-chip). These architectures require high throughput and performance to transfer data in a multicore SoC. Therefore, the NoC (network-on-chip) can be proposed to solve this requirement, but it derived new problems such as power consumption and area. With advancement in the nanometer era, number of cores in a single chip and associated communication complexity are increasing rapidly. To achieve high communication efficiency, network on-chip (NoC) has been proposed.

In NoC, communication among various cores is achieved through on-chip micro-network components (such as switches and network interfaces), instead of the traditional non-scalable buses. NoCs can be designed using either regular or application-specific network topologies. For regular topologies, some existing NoC solutions assume a mesh architecture. Although standard topologies can easily be implemented and also ensure the regularity of the on-chip network, they might not be the best choice for application-specific network-on-chip (ASNoC) due to mismatch between the topology and the application characteristics. Custom topologies are needed to handle the challenges in terms of irregular core sizes, the header flit has PE priority, source address, destination address, and so forth [1, 2]. The NoC synthesis procedure assigns exactly one router to each core.

The routers are placed at a subset of possible router positions, given as input. Links needed to accomplish communication between cores are identified, satisfying link-length constraint LMAX. The overall communication cost of the NoC is defined to be the sum of communication costs for each pair of cores in it [3]. For a pair of cores ci and cj, the communication cost is the product of the bandwidth requirement of their communication and the hop distance between their associated routers. The routers are to be placed, such that, this overall communication cost is minimized. We also consider that the individual routers are much smaller in size than the cores. This assumption is supported by James, in which it has been observed that, on an average, the entire NoC places an area

