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Effective Gasp Pipelining Architecture Based on Constructed Critical Data Path

[1]Dinesh Babu K and [2]Dr. S. Dharmalingam

[1]HOD/Assistant Professor, Department of Electronics and Communication Engineering, Adhi College of Engineering and Technology, Kanchipuram.
[2] Dean, Rathinam Technical Campus, Coimbatore.

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Address For Correspondence:
Dinesh Babu K, HOD/Assistant Professor, Department of Electronics and Communication Engineering, Adhi College of Engineering and Technology, Kanchipuram.

ABSTRACT

The GasP family of asynchronous circuits has been sought for its potential advantages of ultra-high performance and low power especially in the processor and the network on chip (NoC) domains. However, the use of these circuits is currently limited to custom design where extensive SPICE simulations are required to verify timing correctness and performance. In order to incorporate these circuits in the standard ASIC designs, it is essential to establish a more efficient CAD flow.A fully automated characterization flow for developing timing libraries of single track circuit. This thesis extends that flow to the GasP family of circuits and addresses the issue.

KEYWORDS: Index terms- GasP, NOC, Asynchronous domino

INTRODUCTION

During the last decade, there has been a revival in research on asynchronous technology. Along with the continued CMOS technology scaling, VLSI systems become more and more complex. The physical design issues, such as global clock tree synthesis and top-level timing optimization, become serious problems. Even if technology scaling offers more integration possibilities, modularity and scalability are difficult to be realized at the physical level. Asynchronous design is considered as a promising solution for dealing with these issues that relate to the global clock, because it uses local handshake instead of externally supplied global clock was per the work [1-2].

The increasing power consumption and growing complexity of synchronous designs has led to a great deal of interest in asynchronous circuits. The presence of a single global clock in the synchronous designs has resulted into problems like clock tree synthesis, gated clocking design, hold time fixing, and clock skew management. As a result of this, Globally Asynchronous and Locally Synchronous (GALS) systems are gaining prominence.

The GALS systems have shown several advantages including low power in the design of networks on chip (NoCs).

ARM and Sun Microsystems have already been exploring the designs of highly efficient processors using asynchronous templates. ARM worked with Handshake Solutions for the development of ARM996HS which is industry's first clock less processor was per the work [2-5]. The ARM996HS is targeted towards low power applications in the biomedical and the automotive fields. ovalidating the timing performance of these non-standard circuits using static timing analysis. We first discuss some of the relative timing constraints that were identified to ensure the desired working of the GasP control circuits.Then we discuss the characterization flow

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