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A New Zeta Bridge Less Power Factor Correction Converter with Multiple Outputs for Power Quality Improvement in Computer Power Supply System

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ABSTRACT

Reduced power quality, poor output voltage regulation, deliberate dynamic response, input current with high Total Distortion Harmonics (THD) and transients are the foremost problems which are often come across the conventional switched mode power supply (SMPS) used in computers. To diminish these problems, it is suggested here to use a single phase bridgeless ac to dc Power Factor Correction (PFC) converter based on zeta topology at the front end of an SMPS. As input diode bridge is absent and current flows only through two semiconductor switches during each switching cycle, the conduction losses are reduced. The bridgeless zeta at the front end gives firmly regulated output dc voltage even under numerous input voltage changes and loads. The output of the front end converter is connected to a half bridge dc-dc converter for gaining different dc voltage levels at the output that are required in a computer. It is possible to control all the other dc output voltages by controlling a single output voltage. The suggested power supply is simulated using MATLAB Simulink tool and results are presented to validate the performance of this system in enhancing power quality.

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1. INTRODUCTION

All the electronic appliances are supplied from the utility uses the conventional method of ac-dc conversion which contains the diode bridge rectifier (DBR) with a large electrolytic capacitor. As this capacitor

is charged and discharged uncontrollably results in drawing harmonics rich current form utility and goes against the international power quality (PQ) standard limits [1-2]. The recent ac-dc converters combined with power factor correction (PFC) and lessening of harmonics current at the point of common coupling (PCC) recovers the voltage regulation and efficiency at the load side [3-5]. Computers are widely used electronic equipment which is cruelly affected by the problem of PQ.

To maintain the harmonics current within the limit and to obtain the firmly regulated output voltage, one stage or two stage conversion of ac-dc have been recently used in computers. One stage power conversion is very simple, compact and low cost. But it is severely affected by the deliberate dynamic response, complexity of control, high components stress and high capacitance value. Hence conversion of ac into multiple dc voltages by two-stage conversion is widely preferred in computers [6]. Though the requirement of components is high in two-stage conversion rather than one stage, it produces the better output voltage regulation, fast dynamic response and avoids the requirement of large capacitors at the load side. In order to provide PFC and better output voltage regulation, several front-end converters were employed in the power supplies. A boost converter is a general choice for providing PFC in power in power supplies. However, due to its huge input voltage range, it is not preferred choice in computer power supplies [6]. The output voltage of boost converter cannot be controlled less than 300V for a 230V ac input supply and so the buck-boost converter is favored in computers where an extensive variation of input voltages and load are expected [8-9].

The efficiency of two-stage conversion is lesser than that of one stage conversion; to overcome this problem a new bridgeless front end zeta converter is suggested in this paper for computer power supplies. The removal of DBR results in lessened conduction losses and great output voltage range with improved efficiency [10-13]. At the output of the front end zeta converter, a half bridge converter is connected which gives isolation, voltage regulation and multiple dc output voltage which is required for computer power supplies [14-16].

It is perceived from various literature surveys that the research on power quality enhancement in SMPSs using bridgeless PFC converter has not been concentrated much by many researchers so far. In this work bridgeless front end, zeta PFC converter operates in continuous conduction mode (CCM) is used. Test results of the suggested multiple output SMPS are found to be good in line with the simulation performance showing its enhanced power quality and output voltage regulation.

2. SUGGESTED BRIDGELESS ZETA CONVERTER AND CONTROLLER

A. Circuit Configuration

This paper suggests a bridgeless PFC circuits based on zeta topologies operates at continuous conduction mode (CCM) with low switching losses, as shown Figure 1. Zeta converter provides some advantages in PFC applications rather than boost converter, such as simple in implementing transformer isolation, essential inrush current control during starting and overload conditions, reduced input current ripple. The circuit operation during positive and negative half cycle for suggested bridgeless zeta converter of Figure 1 is shown in Figure 2(a) and Figure 2(b), respectively. Referring to the Figure 2, there are one or two switches are in current flow path, therefore switching (conduction) losses and the thermal stresses on the semiconductor switches are further reduced and the efficiency of the circuit is improved unlike in conventional boost converter. Furthermore Figure 2 shows that the input ac voltage is continuously connected to the output ground via slow

recovery diodes D_p and D_n. Hence suggested topology do not affect from high common mode EMInoise.

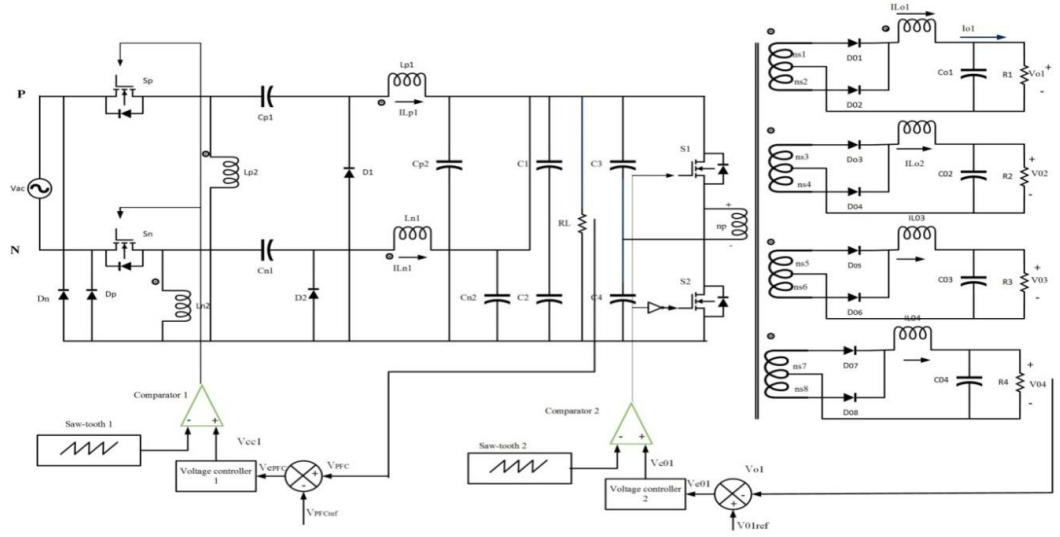

Figure 1. Suggested bridgeless PFC zeta converter with multiple output for computer power supply

This topology comprises of two switches (S_p and S_n) and two diodes (D_p and D_n). Switch S_p and S_n both are driven same control signal which pointedly simplifies the control circuit. The output dc voltage is measured and fed back to the comparator to compare with the reference dc voltage which generates the voltage error signal. This voltage error signal is subsequently given to the proportional-integral (PI) controller and output of PI controller are compared with the high-frequency saw-tooth waveform to produce Pulse Width Modulated (PWM) pulses. This PWM signal is given to both the switches (S_p and S_n). The pulse width is varied based on the PI controller output; therefore output voltage is greatly regulated. This regulated dc output voltage is then fed to the isolated half-bridge converter (second stage) to avail multiple isolated controlled output voltage. The isolation is achieved by the multi-winding high-frequency transformer. All the secondary windings are controlled through one control loop. The upper rated secondary winding of the transformer is chosen for voltage sensing and fed to another comparator to compare with the reference voltage and generated error voltage is fed to PI controller. An output of PI controller is compared with the high-frequency saw-tooth waveform to generate the second set of PWM signals for the half-bridge converter switches S_3 and S_4. A great care has been taken to make sure of sufficient dead time between turning off S_3 and turning on of S_4 in order avoid shoot-through. If a load of any one of the four windings is changed, there will be a corresponding change in the duty cycle to ensure that the controlled output voltage.

B. Working Principle of Front-End Zeta Converter

During the positive half cycle of the input ac voltage the front end zeta converter operates as shown in the Figure 2(a) and current flows through the active components P - S_p – C_{p1} – L_{p1} – R_L – D_p – N, which connects input ac positive half cycle to the load resistor R_L and energy stored in the inductor Ln1during previous negative

half cycle will be discharged and free- wheeling through $Ln_1 - R_L - D_2$, which adds inductor current I_{Ln1} with input ac current I_{ac} (positive half cycle current) and boosts up the converter dc output voltage to the required level.

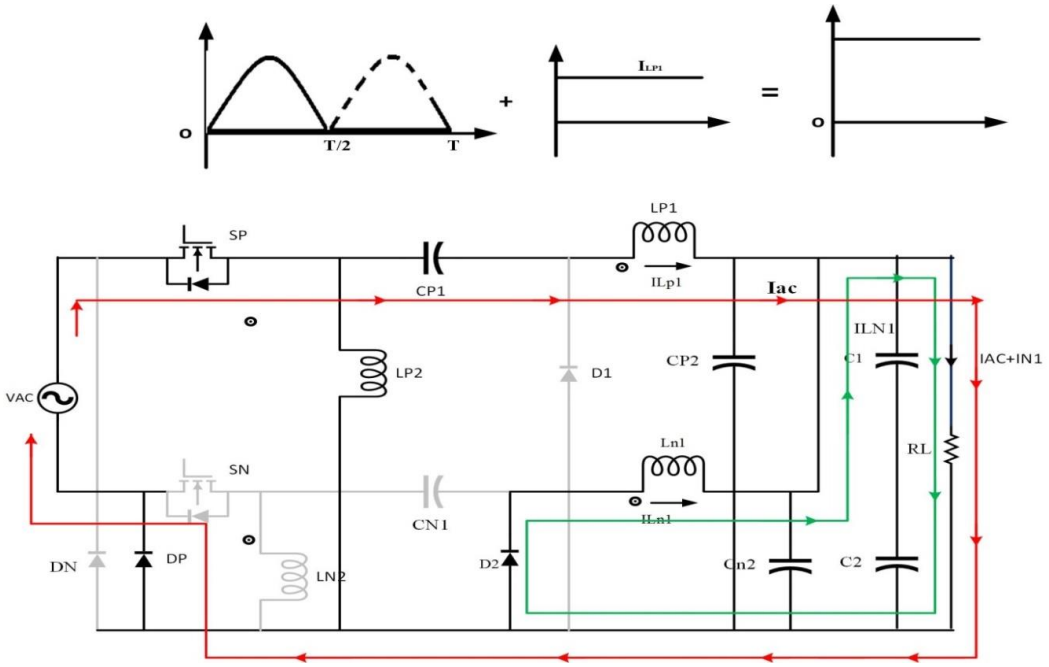

Figure 2(a) Equivalent circuit for the rectifier during positive half cycle

During the negative half cycle the current flows through the active components $N - S_n - C_{n1} - L_{n1} - R_L - D_n - P$, which connects input ac negative half cycle to the load resistor R_L and energy stored in the inductor L_{p1} during the previous positive half cycle will be discharging and free-wheeling through $L_{p1} - R_L - D_1$, which adds inductor current I_{Lp1} with input ac current I_{ac} (negative half cycle current) and boosts up the converter dc output voltage to the required level as shown in Figure 2(b).

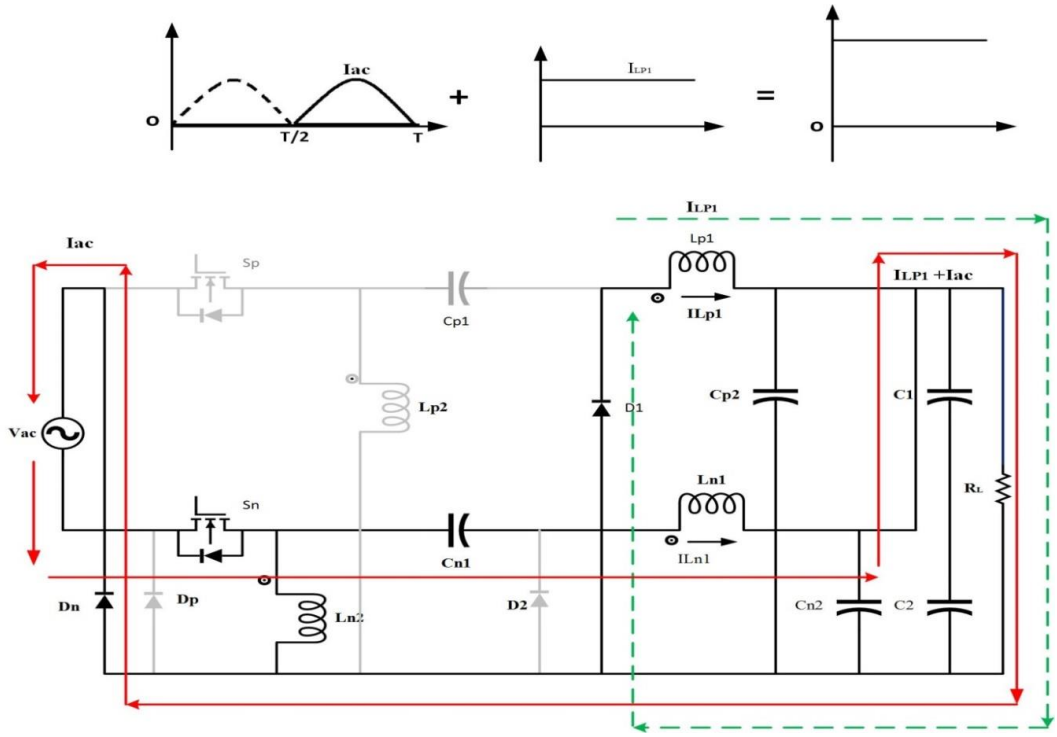

Figure 2(b) Equivalent circuit for the rectifier during positive half cycle

C. **Working Principle of Isolated Converter**

Two high-frequency semiconductor switches are switched on and off interchangeably in one switching cycle. Therefore the converter operation in one half of the switching cycle is similar to that of another half cycle. During the first half cycle switch, S_1 is switched on and diodes on the secondary side of the transformer start conducting and the inductors in all the secondary windings start storing energy. To maintain the dc output voltage constants all the filter capacitor will be discharging through the loads. During the next half cycle the switch S_1 is switched off. The diodes in the secondary side are become forward bias to free-wheel the inductors currents.

3. Design of suggested PFCbridgeless zeta converter

The design of positive and negative operated PFC front end zeta converter is carried out here the average voltage V_{avac} is calculated as,

The duty cycle α of PFC zeta converter is expressed as

$$V_{avac} = \frac{2\sqrt{2}V_{ac}}{\Pi} = \frac{2\sqrt{2}*230}{3.14} = 207 \text{ V}$$

$$\alpha = \frac{Vpfc}{Vpfc+Vavac} = \frac{300}{300+207} = 0.52$$

Regardless of variant in the input voltage from 170V to 270V the output voltage is maintained constant at 300V. Then the duty cycle is calculated for the following value of supply voltage

$\alpha(V_{170}) = 0.63$, $\alpha(V_{200}) = 0.6$, $\alpha(V_{220}) = 0.57$, $\alpha(V_{250}) = 0.54$, $\alpha(V_{270}) = 0.52$ respectively.

Therefore if there is any change in output voltage an error signal is generated at comparator in the PFC control circuit (control circuit 1) by comparing with the reference voltage and it produces corresponding error signal as shown in Figure 1. This error signal is then given to the PI controller, which controls the switch S_p and S_n and tries to maintain the converter DC output voltage constant. Then the isolated converter is controlled by control circuit 2 and it converts DC supply from zeta converter into AC supply and the output of isolated converter is given to the multi secondary transformer in order to get multi-output voltage which is required for computer supply application after converting into DC supply by a corresponding rectifier connected to each transformer secondary winding. This different DC power supply is then taken for computer power supply application.

The input voltage and current of the PFC converter (Zeta converter) are

$I_{in}(t) = I_1 \sin(\omega t)$ (1)

$V_{in}(t) = V_1 \sin(\omega t)$ (2)

Hence $I_1 = \frac{2P0}{Vi\eta}$ (3)

Where P_0 and is the output power and efficiency of the PFC converter. The output current I_0 is dependent on the average inductor current.

$I_L(t) = I_{10}|\sin(\omega t)|$ (4)

$I_0 = \frac{Po}{Vo} = \frac{2}{\Pi} I_{10}$ (5)

WhereI_{10} is an inductor maximum current.

The output capacitor C_1 and C_2:

As the converter input current form is sinusoidal the output voltage ripple is unable to compensate by the converter. Hence the output voltage has its range ruled by average DC component, converter switching

frequency and due to input alternating current. Therefore considering the poorest case, the output capacitors C_1 and C_2 have to compensate the ripple two times of input frequency approximately.

So, as a result

$$C_1 = C_2 = \frac{Po}{4fin\,.\,Vo\,.\,\Delta Vo} = 220\ \mu F. \quad (6)$$

Where;

f_{in} - input frequency;

ΔVo– output ripple.

Semiconductor switches rating (Maximum):

The maximum voltage and current rating of the switches are obtained as follows

$V_{sp,\,sn,\,max} = V_1+V_0$ (7)

$V_{D,\,max} = 2(V_1+V_0)$ (8)

$I_{sp1,}\ I_{sn1\ max} = I_0+I_1+\frac{\Delta ILp1}{2}+\frac{\Delta ILn1}{2}$ (9)

$I_{D1,\,max} = I_0+\frac{\Delta ILp1}{2}$ (10)

$I_{D2,\,max} = I_0+\frac{\Delta ILn1}{2}$ (11)

$V_{sw1,2\,max} = V_{Dp,}\ V_{Dn} = 2(V_{sp,\,sn,\,max})$ (12)

$I_{sw1,2\,max} = I_{Dp,}\ I_{Dn} = 2(I_{sp1,}\ I_{sn1\ max})$ (13)

Where!

V_1, I_1 – Input maximum voltage and current respectively.

I_0 – output current

I_{sp1}, I_{sn1} – current through the switch S_{p1} and S_{n1} respectively

$I_{D1,}$ I_{D2} – corresponding diode current,

$V_{sw1,2\,max}$ - voltage rating of switch S_1 and S_2.

$I_{sw1,2\,max}$ – Current rating of switch S_1 and S_2.

4. SIMULATION RESULT.

The suggested zeta PFC converter is simulated using Matlab Simulink software. Based on the design consideration stated above, the value of main circuit elements are listed in table 1 as shown below.

Table. 1 Component ratings and value of input and output parameters

Zeta PFC converter	Input AC voltage	V_{iac}	260 V
	Inductor	$L_{p1}=L_{p2}=L_{n1}=L_{n2}$	1 mH
	Capacitor	$C_{p1}=C_{n1}$, $C_{p2}=C_{n2}$,	1 μF and 470 μF
	Capacitor	$C_1=C_2$	220 μF
	Output voltage	V_{odc}	440 V
Isolated converter	Output voltage	V_{oac}	220 V
	Capacitor	$C_2=C_3$	2200 μF
Load diode rectifier	Filter	L,C	1mH, 2200 μF
	Load resistor	$R_1 = R_2 = R_3 = R_4$	500 ohm
	Output voltage	V_{01}, V_{01}, V_{01} and V_{01}	5, 12, 25, 38 V

Fig. 3(a) shows the source voltage and current during full loaded condition concurrently. It is observed from this waveform that the source voltage and current both are in phase and practically sinusoidal, further the THD is just 2.21% as shown in Figure 3(b).

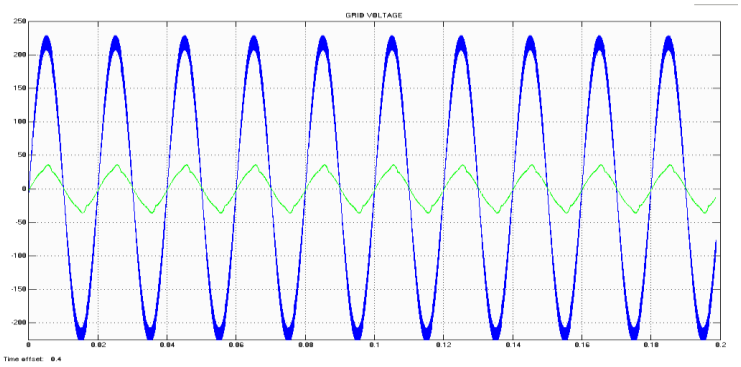

Figure 3(a) Source voltage and current waveform.

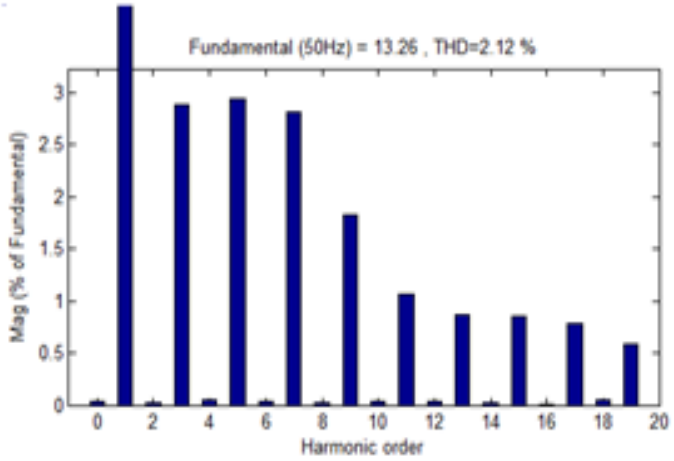

Figure 3(b) Total Harmonics Distortion of source current under full load.

Figure 3(c) shows the boost-up DC voltage by the zeta PFC converter with the magnitude of around 640V and which is fed back to the isolated converter (half bridge inverter) to convert into AC voltage. Figure 3(d) shows the waveform of different DC output voltages (V_{01}, V_{02}, V_{03}, and V_{04} with the magnitude of 5, 12, 25 and 38 V respectively) those are required for computer power supply application.

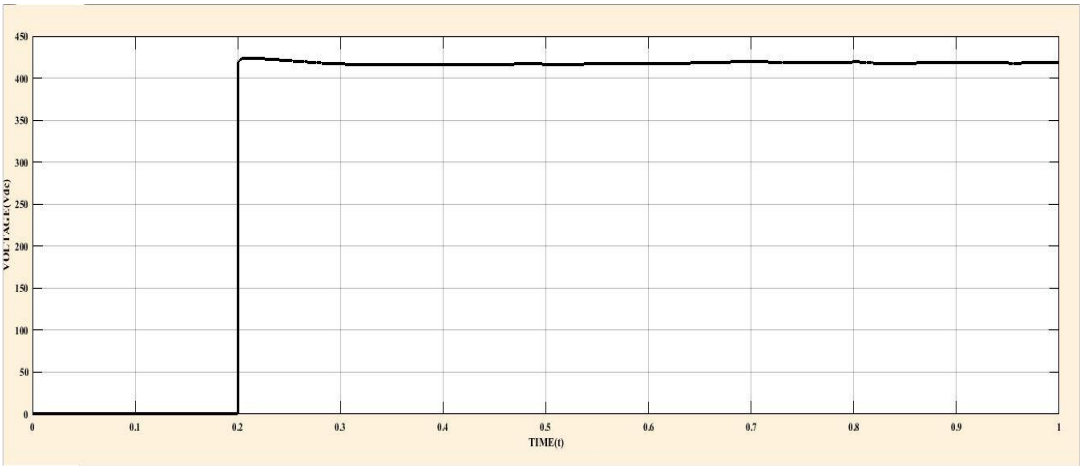

Figure 3(c) Boost-up DC voltage by Zeta PFC converter

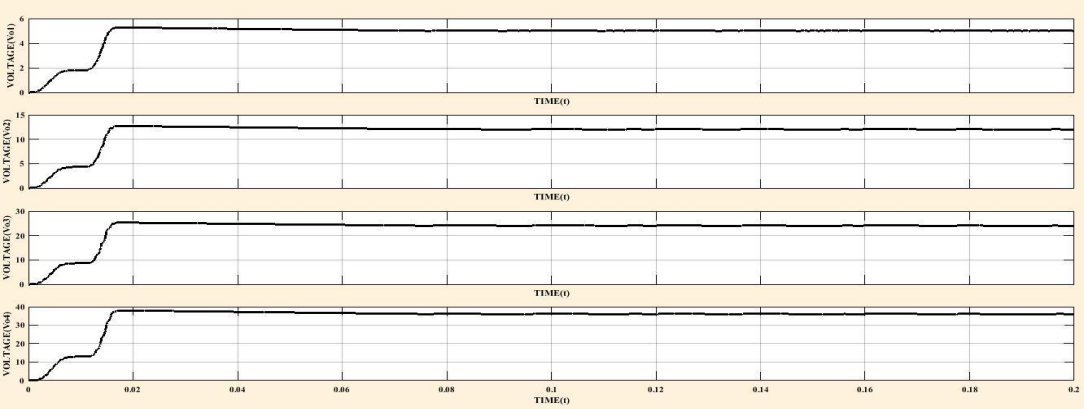

Figure 3(d) Multiple DC output voltage from load rectifier.

5. CONCLUTION

A new zeta PFC converter is introduced in this paper having reduced conduction and switching losses due to the establishment of bridge less converter. The zeta topology presents a good voltage gain and regulation when comparing to a conventional boost converter. The input current and voltage are in phase with each other and practically sinusoidal. This converter configuration is fully examined and simulation results are presented. The power factor is almost near unity and produces reduced THD. Therefore, the suggested system provides the effective solution to the power quality issues at the front end of the switched mode power supply and it can be strongly recommended elucidation for computers and other similar appliances.

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