DESIGN AND ESTIMATION OF SUBTHRESHOLD ADIABATIC LOGIC CIRCUITS FOR ULTRALOW-POWER (UP) APPLICATIONS USING EDA PLATFORM

Abirami. B.M
Department of Electronics and Communication Engineering, Dr.APJ Abdul Kalam Centre for Research,
Adhi College of Engineering and Technology,Sankarapuram - 631605, Tamilnadu, India.
Author's email: abirami.ece@adhi.edu.in

Abstract :

In this paper, a new type of Sub threshold Adiabatic Logic (SAL) based circuit level estimation for High Speed Adder (4-bit Carry-Select Adder) was presented. To achieve ultralow power and to avoid heat dissipation in many modern applications, such as mixed-signal and embedded circuits increased their importance of designing logics in SAL based approach. This is a new concept for fast adder circuits using SAL which will be useful in energy saving applications. By comparing with conventional methods like Static CMOS and Adiabatic logic implementation, this novel scheme shows a significant performance in terms of power consumption, area and energy saving factors. Several parameters of the proposed design were simulated using technology models (180nm, 22nm) in the Tanner EDA tool.

Keywords : Static CMOS, Sub threshold region, Carry-Select Adder (CSLA), Efficient Charge Recovery Logic (ECRL), Sub threshold Adiabatic Logic (SAL), Tanner EDA.

I. INTRODUCTION

This paper proposed a SAL based fast adder design (4-bit CSLA) and it has been analysed with previous techniques of logic implementation like standard CMOS, adiabatic and SAL based existing 4-bit carry lookahead adder. The aim is to improve the ultralow power achievement in sub or near threshold region of logic designs. The effectiveness of the proposed scheme works good in key metrics such as power and energy consumption, required area and avoid heat dissipation. In addition to this concept, future enhancement for designing logic circuits in subthreshold region with reversible logic styles and study of this logic with respect to VLSI boards. Hearing aids and pacemakers, personal digital assistants, laptops, medical, self power devices and energy saving embedded circuits are the applications in which the proposed method used.

II. SURVEY ON RELATED WORK

Study of ramping signals based on adiabatic and subthreshold concepts [1] is important. Various adiabatic logic families like ECRL, PFAL (Positive Feedback Adiabatic Logic) analysed and tradeoffs [2] between energy consumption, area. Conventional and energy savings technique based VLSI applications designed thereby studying various performance metrics like voltage, power, area, temperature, frequency etc. [3]. Implementation of CSLA using adiabatic logic and computing area, power & other factors [4]. Concepts involved in adiabatic logic to design low power dissipation full adder [5]. All concepts related with energy recovery in irreversible manner [6]. Multiplexers design using clocked adiabatic logic [6]. Types of implementations such as static and adiabatic for multiplexer circuits has been studied [7].

Theoretical concepts: adiabatic designs and its principles and example [8]. Noise, power analysis of adiabatic styles was proven to be good compared to static logics [9]. Application based study and implementation of ultralow power sub threshold circuits [10]. Basics of different adiabatic designs and its application oriented uses [11]. Concepts of Complimentary pass transistor logics based multipliers [12]. For designing new type adder circuit, the previous work related to each adiabatic style should be studied on various key criteria's [13]. Positive feedback logic based cmos circuits provide good noise margin and energy saving ratio [15]. While considering Sequential circuits, it has been compared using reversible and irreversible generalizations [16]. Controlling static power dissipation when the system is idle and not performing any operation is explained by power gating techniques [17]. A decoder circuit has been examined using various CMOS technology models based on standard CMOS design compared with adiabatic style [18]. Multipliers performance using partial adiabatic logics has been studied [19]. Comparison: conventional and reversible logics for reduction of static power [20]. Concepts of digital circuits under subthreshold for biomedical applications [21]. All studies regarding circuits performing based on subthreshold concepts [22]. The adiabatic based adders for energy efficient designs are very much useful in future [23]. Energy recovery logics: implementing full adder designs to achieve low power has been compared with my proposed work [24].