International Journal of Applied Engineering Research, ISSN 0973-4562 Vol. 10 No.87 (2015)

LOW POWER AND AREA EFFICIENT DCT ARCHITECTURE BY USING ELIMINATION METHOD IMPLEMENTED IN IMAGE PROCESSING

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Abstract: A wide interest has been observed to find a low power and area efficient hardware design of DCT algorithm. The proposed a novel CSE based pipelined architecture for DCT aimed at reproducing the cost metrics of power and area while maintaining high speed and accuracy in DCT applications. The proposed design combines the techniques of CSD representation and CSE to implement the multiplier less method for fixed constant multiplication of DCT coefficients. Furthermore, razor flip flop used to reduce timing errors. Moreover, this design meets the real time constraints of different video/image coders and peak-signal-to-noise-ratio (PSNR) requirements. Furthermore, the proposed technique has significant advantages over recent well-known methods along with accuracy in terms of power reduction, silicon area usage, and maximum operating frequency.

INDEX: Discrete Cosine Transform,Cannonical Signed Digital Representation, Common Sub expression Elimination

1.INTRODUCTION

In the modern era, digital image processing has become widely used in electronic devices. A plethora of different multimedia applications spread rapidly, such as camcorders, cameras, video conferencing on mobile phones, online video streaming, video surveillance, patient monitoring systems, and high definition television (HDTV). These applications require a large amount of data to represent the digital images, resulting in large memory and transmission costs. Modern compression techniques play an important role to reduce the high storage and transmission cost. Image processing techniques have become more significant for various multimedia applications in embedded systems. Speed, power consumption, hardware area, resource usage, and throughput are the main criteria to be concerned in the development of image processing algorithm architectures. Especially, in portable systems, the key features are low power and low area with speed.Thus, it has been the field of interest for the researchers.

Discrete cosine transform (DCT) is widely used in the majority of the international video/image standard coders. In the recently published work, various high throughput DCT architectures have been designed to meet the requirement of real time applications . DCT is one of the compute intensive parts in various image/video coding standards, such as JPEG(Jointed Photographic Practiced Group), H.261,H.263, and H.264/MPEG (Motion Pictures Practiced Group). DCT transforms a signal or image from the spatial domain to the frequency domain. In emerging multimedia applications, DCT is widely used in portable systems, as they have limited CPU computing ability. Hence, it requires efficient hardware which consumes low power and low area and also satisfies the throughput criteria of the coder. In this paper, a novel architecture is proposed for DCT computation. It is based on the Canonical Signed Digit (CSD) encoding and use of Common Sub expression Elimination(CSE) technique. The efficient use of the CSE, not only in CSD encoding, but also in intermediate DCT coefficients, is introduced to compute the DCT results. Due to this approach, multiple identical sub expressions are needed to compute only once, which reduces the resources usage because of sharing the sub expressions. As a result, the total number of adders/subtractors required to compute DCT is reduced.