

## AN EFFICIENT FPGA DESIGN OF FACE RECOGNITION SYSTEM

**A. PANIMALAR,**

Department of Electronics and Communication Engineering, Dr.APJ Abdul Kalam Centre for Research,  
Adhi College of Engineering and Technology, Sankarapuram - 631605, Tamilnadu, India..  
Email: [panimalar.ece@adhi.edu.in](mailto:panimalar.ece@adhi.edu.in)

### Abstract:

In this paper, a new type of face recognition system has been implemented in FPGA. The main blocks used to design real-time face recognition system involves face detection, face recognition and down sampling module. The proposed method uses viola-jones and eigenface algorithm for making the system flow that is reading input video from camera, detection of face locations and recognise each face based on which the output results will be displayed. The entire system provides an operating range of 45 frames per second and it is implemented on a Virtex-5 FPGA board.

**Keywords.** Face Recognition; Eigenface; Complete face recognition system; face detection; FPGA; real-time processing.

## 1. INTRODUCTION

Various face detection and face recognition algorithms has been researched and more challenging area in terms of both software and hardware [6] [1] [4] [5] [7] [3]. In past decades, different face recognition algorithms have been developed [1] [5]. All hardware part involving this face recognition system will take unknown face image as input [4] [11]. Currently the face recognition systems not accept if the input is not face image [12]. Hence, the proposed framework contains both a face detection to find and face recognition to identify the unknown face image. Eigenface algorithm is used by face recognition subsystem [2]. First video data from camera is sending to face detection and the frames send to face recognition via downsampling. Proposed method identifies or verifies a person automatically. The design has been implemented on FPGA using pipelined and non pipelined structures. The performance analysis between software and hardware was estimated. Integration of downsampling with face recognition and detection has been discussed in the proposed work.

## II. FACE DETECTION AND RECOGNITION SUBSYSTEM

Fig. 1 shows the complete face recognition system. It consists of following steps:

**Image reader** - In this module, image frame buffer stores each pixel of unknown image by reading 20×20 image. Recognize pixels for the unknown image needs to be done.

**Normalized Image calculator** - It starts the normalized image calculation. Difference between average and the input image is determined. Normalized image is obtained by subtracting average image with input image pixels.

**Weight Vector Finder** - Computationally expensive step. It finds weight values for input image and Eigenvector values are ready by eigenface reader.

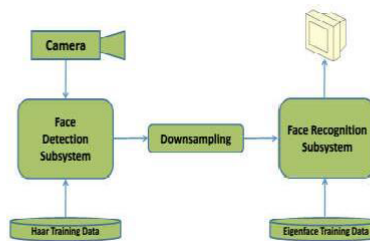


Fig. 1 – Face Detection and Recognition Block diagram of the overall process