ISSN 2321-807X
Volume 13 Number4
Journal of Advances in chemistry

Performance Analysis of Low Power Encoding Technique for Multi Port Network On-Chip Router

R. Anitha[1,*] C. SenthilSingh[2]
Associate professor Adhi college of Engineering and Technology
anithagodavarthy@gmail.com
Professor Adhi college of Engineering and Technology
senthilsingh@gmail.com

ABSTRACT

Network on chip (NoC) router plays an important role in packet forwarding from router to network interface module. In this paper, a low power packet encoding technique for multi port network on chip router is designed. The proposed packet encoding technique consists of table mapper unit and differential coding unit. The table mapper unit is used to encode the address and control signals of the packet and differential coding unit is used to encode the data flits in the packet. **The proposed methodology is tested on different Virtex family and achieved 26.79mW of power consumption.**

Keywords

Routing, Network on chip, Table mapper, Encode, Power consumption

1. INTRODUCTION

The process of finding the geometric layout of all nets is defined as routing. The most important goal of routing is the reduction of area of an IC chip and the most important objective of routing is to complete all the required connections. Otherwise, the chip would not function well and may even fail. In general, Very Large Scale Integration (VLSI) routing is an important design step in the sense that the quality of routing solution has great impact on various design parameters such power consumption, circuit timing, chip consistency, manufacturability, etc. The inputs of the general routing problem are Net list, RC delay per unit length on each network layer, as well as for each type of medium and timing budget for critical nets.

Routing is typically a very complex combinatorial problem. To make it manageable, the routing problem is usually solved by two steps– Global Routing and Detailed Routing. Global routing first partitions the routing region into global routing cells and decides the path by global routing grid graph. Generally it can be solved much faster than detailed routing. Detailed routing takes the output from the global router and produces an accurate geometric design of the wires to connect the blocks.

To make it easier for the routing problem, the routing regions are divided into rectangular blocks. The blocks contain pins which need to be connected in their perimeter. There are two types of routing regions: Channel and switchbox. A channel is rectangular area which has two open ends and other two sides are bounded by two opposite sides of the blocks. Channel routing has been used to implement the layout of Integrated Circuits (ICs) in a variety of design styles such as gate arrays, standard cells, and macro-cells (building blocks).

In this paper, we mainly focus on methods to reduce the power dissipation by the network links. The power dissipation due to the network links depends on the power dissipated by routers and network interfaces (NIs). Section 2 discusses the related works in brief, while Section 3 presents an overview of the proposed router scheme and its implementation. Section 4 depicts the results and discussion of the proposed routing scheme and its comparison with that of other approaches. Finally, this paper is concluded in Section 5.

2. RELATED WORKS

Sowmya et al. (2013) provided a onetime networking solution by means of merging the VLSI field with the networking field. Networking router today are with minimum pins and to enhance the network we go for the bridging loops which effect the latency and security concerns with protocol switching technique embedded in the router engine itself. This paper is based on the hardware coding which gave a great impact on the latency issue as the hardware itself will be designed according to the need. They provided a multipurpose networking router by means of Verilog code with which the same switching speed with more security is maintained. Their paper mainly focused on the implementation of hardware IP router which processes multiple incoming IP packets with different versions of protocols simultaneously with the purpose of increasing switching speed of a routing per packet for both the current trend protocols.

A heuristic approach to find the optimal routing path and buffer location simultaneously for minimal interconnect delay was presented in Khan et al. (2013) and in Avob et al. (2010), Prim's Algorithm was modified and implemented as a principle of finding the cost of the RSMT. Dong et al. (2009) proposed a routing algorithm based on improved Discrete PSO in which a novel encoding for DPSO and update functions are performed to find the RSMT. The results of these methods [2–4] were compared with conventional methods and proved to give a better routing optimization.

In Stan et al. (1995), the number of transitions from 0 to 1 for two consecutive flits is counted. If the number is larger than half of the link width, the inversion will be performed to reduce the number of 0 to 1 transitions when the flit is transferred through the link. This method deals with only self-switching neglecting the coupling switching.