




ADHI

COLLEGE OF ENGINEERING & TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING FACULTY PROFILE

NAME		Dr.J.KALAIVANI					
DESIGNATION		ASSOCIATE PROFESSOR					
DEPARTMENT		COMPUTER SCIENCE AND ENGINEERING					
MAIL ID	kalaivani.cse@adhi.edu.in		CONTACT NO	9790273451			
EDUCATIONAL QUALIFICATION							
Category	Name of the degree	Specialization	Year of Passing	Name of the College	Name of the University		
UG	B.E	CSE	2005	National Engineering College, Kovilpatti	Anna University		
PG	M.E	CSE	2008	Mepco Schlenk Engineering College, Sivakasi	Anna University		
PhD	Ph.D	Computer Networks	2017	Madras Institute of Technology, Chromepet	Anna University		
PROFESSIONAL EXPERIENCE							
Name of the College		Designation	Joining Date	Relieving Date	Experience		
					Years	Months	Days
TOTAL					8	6	



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Areas of Interest/ Specialization	Computer Networks, Operating Systems, C,C++, Object Oriented Programming, Data Structures
NO.OF PAPER PUBLISHED	4
Journal	2
Top 5 International Journals Published	International Journals-2 <ol style="list-style-type: none">Kalaivani, J & Vinayagasundaram, B 2016, 'Deadlock Free Load Balanced Adaptive Routing for Network on Chip (NoC) Systems', Journal of Computational and Theoretical Nanoscience (JCTN), vol. 13, no.10, pp.7592-7598, ISSN:1546-1955 (Print): EISSN: 1546-1963.Kalaivani, J & Vinayagasundaram, B 2013, 'K-Step Look Ahead in Load Balanced Adaptive Routing for Network on Chip (NoC) Systems', International Review on Computers and Software (IRECOS), vol. 8, no. 6, pp. 1271-1278, ISSN: 1828-6003.
Conference	International Conference-2 <ol style="list-style-type: none">Kalaivani, J & Vinayagasundaram, B 2016 April, 'Energy aware scheduling and dynamic job mapping algorithm for Network-on-Chip architectures', In Recent Trends in Information Technology (ICRTIT), 2016 International Conference on, IEEE. pp.1-4.



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	<p>2. Kalaivani, J & Vinayagasundaram, B 2013, 'Load balanced adaptive routing with reduced overhead for Network on Chip (NoC) Systems', In Information Communication and Embedded Systems (ICICES), 2013 International Conference on, IEEE. pp. 893-898.</p>
NO.OF WORKSHOP ATTENDED	9
NO.OF EVENT ORGANIZED	2
PROJECTS GUIDED	
❖ UG Level	2